CLAIMS

What is claimed is:

1. A method for verifying the validity of transmitted digital information data bits arranged in one or more data packets comprising:

performing a cyclic redundancy check on said one or more data packets to obtain a check sequence for each said one or more data packets; and

condensing said check sequences into a single reduced bit count check sequence equivalent; and

wherein the number of bits occupied by said reduced bit count check sequence equivalent is fewer than the number of bits occupied by said check sequences, thus freeing additional data bits for use by digital information data bits.

2. The method of Claim 1, further comprising:

transmitting said reduced bit count check sequence equivalent and said data packets;

receiving said reduced bit count check sequence equivalent and said data packets;

performing said cyclic redundancy check on said received data packets to obtain received check sequences;

condensing said received check sequences into a single reduced bit count received check sequence; and

comparing said reduced bit count received check sequence with said reduced bit count transmitted check sequence to determine if said data packets were transmitted accurately.

3. The method of Claim 2, further comprising:

retransmitting any of said data packets transmitted with errors.

4. The method of Claim 1, wherein said condensing step is performed by an error correction code.

5. The method of Claim 1, wherein said data packets comprise multiple data packets within a superframe.

6. The method of Claim 1, wherein said data packets comprise stand-alone data packets.

7. The method of Claim 1, wherein said data packets comprise multiple data packets.

8. A data transmission system comprising:

a transmitter operable to perform a cyclic redundancy check on at least one data packet to produce at least one check sequence representing said data packet; and

a condensing device operable to condense said at least one check sequence into a check sequence equivalent that is smaller than said at least one check sequence; and

wherein said at least one data packet and said check sequence equivalent are transmitted by said transmitter.

9. The system of Claim 8, wherein the number of bits occupied by said check sequence equivalent is fewer than a number of bits occupied by said at least one check sequence, thus freeing additional data bits for use as information data bits.

10. The system of Claim 8, further comprising:

a receiving device operable to receive said transmitted data packet and said transmitted check sequence equivalent and operable to perform cyclic redundancy check on said transmitted data packet.

11. The system of Claim 10, wherein said receiving device further comprises:

a forward error correction code device operable to reduce said transmitted data packets into a single reduced bit count received cyclic redundancy check sequence.

12. The system of Claim 11, further comprising:

a comparator for comparing said reduced bit count received cyclic redundancy check sequence with said reduced bit count transmitted cyclic redundancy check sequence to determine whether said at least one data packet was received by said receiver in substantially the same condition as transmitted by said transmitter.

13. The system of Claim 8, wherein said condensing device comprises a forward error correction code.

14. The system of Claim 11, wherein said forward error correction code device comprises a block code.

15. The system of Claim 8, wherein said at least one data packet comprises a plurality of data packets associated with a single superframe.

16. The system of Claim 11, wherein said data packets that are received by said receiver in a condition different then transmitted by said transmitter are re-transmitted from said transmitter to said receiver.

17. A method for verifying the validity of transmitted digital information data bits arranged in one or more data packets comprising:

performing a cyclic redundancy check on said one or more data packets to obtain a check sequence for each said one or more data packets;

condensing said check sequences into a single reduced bit count check sequence equivalent, wherein the number of bits occupied by said reduced bit count check sequence equivalent is fewer than the number of bits occupied by said check sequences, thus freeing additional bits for use as information data bits;

transmitting said reduced bit count check sequence equivalent and said data packets;

receiving said reduced bit count check sequence equivalent and said data packets;

performing said cyclic redundancy check on said received data packets to obtain received check sequences;

condensing said received check sequences into a single reduced bit count received check sequence; and

comparing said reduced bit count received check sequence with said reduced bit count transmitted check sequence to determine if said data packets were transmitted accurately.

18. The method of Claim 17, wherein both of said condensing steps are performed by a forward error correction code.

19. The method of Claim 17, wherein said data packets comprise a superframe.

20. The method of Claim 19, further comprising:

retransmitting any of said data packets transmitted with errors.

21. The method of Claim 19, further comprising:

Identifying said data packets that are transmitted with errors so that said data packets with errors can be further processed.